REMARKS

I. Introduction

In response to the Office Action dated September 6, 2002, claims 1-10 have been amended, and claims 11-13 have been added to the application. Claims 1-13 are present in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested. It is not the applicant's intent to surrender any equivalents due to the amendments presented herein.

II. Art-Based Rejections

In paragraphs 1-2 of the Office Action, claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stevens (USPN 6,173,345).

The Applicants respectfully traverse the rejections in light of the amendments above and the arguments below. Specifically, the cited art does not teach nor suggest the limitation of outputting delay adjustment signals based on the data signals as claimed in the present invention.

A. The Stevens Reference

The Stevens reference discloses a method and apparatus for levelizing transfer delays for a channel of devices. See Abstract. A driver circuit 242 is coupled to the core 243 to drive data from the core 243 to the data bus 234. The driver 242 is enabled or strobed by an output from the variable delay circuit 244 which is in turn controlled by a delay register 249. The delay register 249 is coupled to serial control logic 248, and therefore may be programmed with device delay values determined by the BIOS and transmitted by the memory controller 200 via the serial control logic 224 and serial bus 236. See Col. 5, lines 34-43.

B. The Claims are Patentable over the Cited Art

Claims 1-13 recite semiconductor integrated circuit devices with delay adjustments. Specifically, a semiconductor integrated circuit device in accordance with the present invention comprises register circuits which receive data signals,

where an output timing of each of the register circuits is controlled by a clock signal. The device further comprises a delay adjustment signal output circuit which receives the data signals and outputs delay adjustment signals based on the data signals, delay adjustment circuits which receive outputs of the register circuits and output delay adjusted data signals, where a delay time of each of the delay adjustment circuits is adjusted based on the delay adjustment signals, and driver circuits which receive the delay adjusted data signals.

The cited art does not teach nor suggest the limitation of outputting delay adjustment signals based on the data signals as claimed in the present invention.

The Stevens reference specifically shows that the delay register 249 is coupled to serial control logic 248, and is programmed with device delay values determined by the BIOS and transmitted by the memory controller 200 via the serial control logic 224 and serial bus 236, and not controlled by the data signals as recited in the claims of the present invention.

The present invention allows for the use of data signals to control the delay time of each of the delay adjustment circuits, which is not contemplated, suggested, or taught by the cited art. This improvement over the prior art allows for more flexible system architectures and devices.

The novel elements, as claimed in independent claims 1, 5, and 7 of the present invention, is not taught nor suggested by the cited references, and, as such, the claims of the present invention are patentable over the cited references.

Further, dependent claims 2-4, 6, and 8-13, in addition to containing the novel elements of independent claims 1, 5, and 7, recite additional novel elements and functions which further distinguish them from the cited references.

IV. Conclusion

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectively solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,
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APPENDIX A: SPECIFICATION AND CLAIMS IN MARKED-UP FORM

IN THE SPECIFICATION

Please amend page 13, lines 10-13, as follows:

A1

As shown in FIG. 4, TFG31-1 comprises, for example, PMOS P1 and [PMOS N1] NMOS N1 mutually connected in parallel between the input terminal Vin and the output terminal Vout.

Please amend page 14, lines 16-17 as follows:

A2

As shown in FIG. 5, the DEC comprises an exclusive [AND] OR circuit (hereinafter referred to as EXOR) 51.

IN THE CLAIMS

Please amend claims 1-10 as follows:

A3

1. (Amended) A semiconductor integrated circuit device comprising:

[a register circuit which receives a data signal] register circuits which receive data signals, an output timing of [the register circuit] each of the register circuits being controlled by a clock signal;

a delay adjustment signal output circuit which receives the data signals and outputs delay adjustment signals based on the data signals;

[a delay adjustment circuit which receives an output of the register circuit] delay adjustment circuits which receive outputs of the register circuits and output delay adjusted data signals, a delay time of [the delay adjustment circuit] each of the delay adjustment circuits being adjusted [by a delay adjustment signal based on the data signal] based on the delay adjustment signals; and

[a driver circuit which receives an output of the delay adjustment circuit]

the driver circuits which receive the delay adjusted data signals.

2. (Amended) The device according to claim 1, wherein [the data signal is a read data signal, and the driver circuit is an off-chip driver circuit] the data signals are read data signals, and the driver circuits are off-chip driver circuits.

3. (Amended) The device according to claim 1, wherein [the data signal is a write data signal, and the driver circuit is a write data buffer circuit] the data signals are write data signals, and the driver circuits are write data buffer circuits.

A3

4. (Amended) The device according to claim 1, wherein [the data signal is an address signal, and the driver circuit is an address buffer circuit] the data signals are address signals, and the driver circuits are address buffer circuits.

5. (Amended) A semiconductor integrated circuit device comprising:

a delay adjustment signal output circuit which receives data signals and outputs delay adjustment signals based on the data signals;

[a delay adjustment circuit which receives a clock signal] delay adjustment circuits which receive a clock signal and output delay adjusted clock signals, [a delay time of the delay adjustment circuit being adjusted by a delay adjustment signal based on a data signal] delay times of the delay adjustment circuits being adjusted based on the delay adjustment signals;

[a register circuit which receives the data signal] register circuits which receive the data signals] register circuits which receive the data signals, an output timing of [the register circuit being controlled by a clock signal which is delay

adjusted in the delay adjustment circuit] each of the register circuits being controlled by the delay adjusted clock signals; and

[a driver circuit which receives an output of the register circuit] driver circuits which receive outputs of the register circuits.

6. (Amended) The device according to claim 5, wherein [the clock signal is a clock to output a read data, the data signal is a read data signal, and the driver circuit is an off-chip driver circuit] the data signals are read data signals, and the driver circuits are off-chip driver circuits.

A3

7. (Amended) A semiconductor integrated circuit device comprising:

[register circuits which receive data signals, an output timing of each of the register circuits being controlled by a clock signal;

delay adjustment circuits which receive outputs of the register circuits, a delay time of each of the delay adjustment circuits being adjusted by a delay adjustment signal based on the data signals adjacent to each other; and

driver circuits which receive outputs of the delay adjustment circuits.]

a first register circuit which receives a first data signal;

a second register circuit which receives a second data signal;

a delay adjustment signal output circuit which receives the first and second data signals and outputs a delay adjustment signal based on the first and second data signals;

a first delay adjustment circuit which receives an output of the first register circuit and outputs a first delay adjusted data signal, a delay time of the first delay adjustment circuit being adjusted based on the delay adjustment signal;

a second delay adjustment circuit which receives an output of the second

register circuit and outputs a second delay adjusted data signal, a delay time of the second delay adjustment circuit being adjusted based on the delay adjustment signal;

a first driver circuit which receives the first delay adjusted data signal; and

a second driver circuit which receives the second delay adjusted data signal.

8. (Amended) The device according to claim 7, wherein the first and second data signals are read data signals, and the first and second driver circuits are off-chip driver circuits.

A3

9. (Amended) The device according to claim 7, wherein the first and second data signals are write data signals, and the first and second driver circuits are write data buffer circuits.

10. (Amended) The device according to claim 7, wherein the first and second data signals are address signals, and the first and second driver circuits are address buffer circuits.